

27C256 262,144-Bit (32,768 x 8) UV Erasable CMOS PROM Military Qualified

General Description

The 27C256 is a high-speed 256K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The 27C256 is designed to operate with a single +5V power supply with $\pm 10\%$ tolerance. The CMOS design allows the part to operate over Military Temperature Range.

The 27C256 is packaged in a 28-pin dual-in-line package with transparent lid and a 32-pin windowed LCC. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

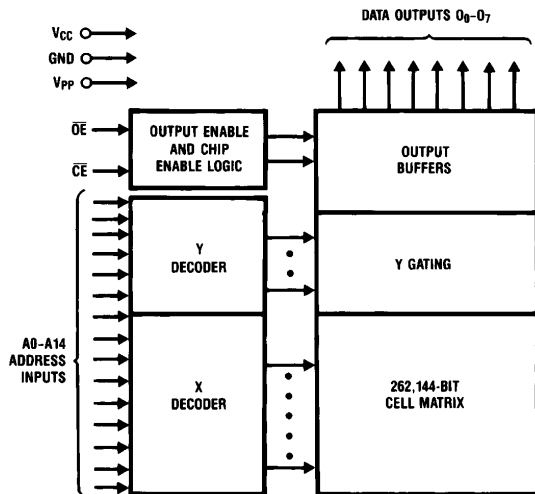
This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

The 27C256 specified on this data sheet is fully compliant with MIL-STD-883, Revision C.

Features

- Clocked sense amps for fast access time down to 250 ns
- Low CMOS power consumption
 - Active power: 55 mW max
 - Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible with NMOS 256K EPROMs
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Windowed DIP and LCC package options
- Specifications guaranteed over full military temperature range (-55°C to $+125^{\circ}\text{C}$)
- This device is processed in compliance with SMD 86063, and the DIP version is dual marked

Block Diagram



TL/D/10332-1

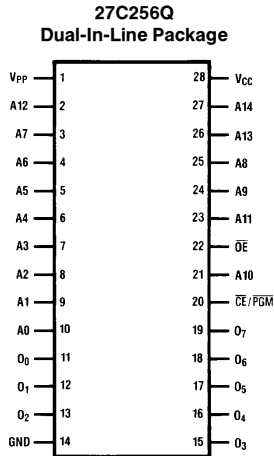
Pin Names

| | |
|--------------------------------|---------------|
| A0-A14 | Addresses |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| O ₀ -O ₇ | Outputs |
| PGM | Program |
| NC | No Connect |

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NSC800™ is a trademark of National Semiconductor Corporation.

Connection Diagrams

| 27C512 | 27C128 | 27C64 | 27C32 | 27C16 |
|--------|-----------------|-----------------|-------|-------|
| 27512 | 27128 | 2764 | 2732 | 2716 |
| A15 | V _{PP} | V _{PP} | | |
| A12 | A12 | A12 | | |
| A7 | A7 | A7 | A7 | A7 |
| A6 | A6 | A6 | A6 | A6 |
| A5 | A5 | A5 | A5 | A5 |
| A4 | A4 | A4 | A4 | A4 |
| A3 | A3 | A3 | A3 | A3 |
| A2 | A2 | A2 | A2 | A2 |
| A1 | A1 | A1 | A1 | A1 |
| A0 | A0 | A0 | A0 | A0 |
| O0 | O0 | O0 | O0 | O0 |
| O1 | O1 | O1 | O1 | O1 |
| O2 | O2 | O2 | O2 | O2 |
| GND | GND | GND | GND | GND |

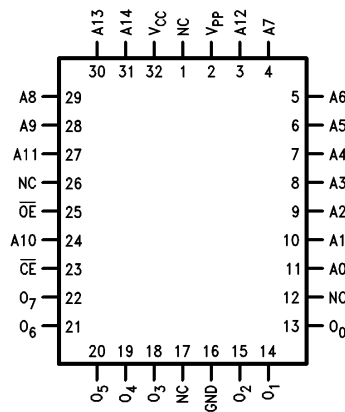


| 27C16 | 27C32 | 27C64 | 27C128 | 27C512 |
|-----------------|--------------------|-----------------|-----------------|--------------------|
| 2716 | 2732 | 2764 | 27128 | 27512 |
| | | V _{CC} | V _{CC} | V _{CC} |
| | | PGM | PGM | A14 |
| V _{CC} | V _{CC} | NC | A13 | A13 |
| A8 | A8 | A8 | A8 | A8 |
| A9 | A9 | A9 | A9 | A9 |
| V _{PP} | A11 | A11 | A11 | A11 |
| OE | OE/V _{PP} | OE | OE | OE/V _{PP} |
| A10 | A10 | A10 | A10 | A10 |
| CE/PGM | OE | OE | OE | OE |
| O7 | O7 | O7 | O7 | O7 |
| O6 | O6 | O6 | O6 | O6 |
| O5 | O5 | O5 | O5 | O5 |
| O4 | O4 | O4 | O4 | O4 |
| O3 | O3 | O3 | O3 | O3 |

TL/D/10332-2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the 27C256 pins.

NS Package Number J28AQ



TL/D/10332-6

Bottom View

NS Package Number EA32CQ

Military Temperature Range (-55°C to +125°C)
V_{CC} = 5V ± 10%

| Parameter/Order Number | Access Time |
|------------------------|-------------|
| 27C256Q250/883 | 250 |
| 27C256Q300/883 | 300 |
| 27C256Q350/883 | 350 |
| 27C256E250/883 | 250 |
| 27C256E300/883 | 300 |
| 27C256E350/883 | 350 |

Absolute Maximum Ratings (Note 1)

| | | | |
|--|--------------------------------------|--|-----------------|
| Temperature Under Bias | -55°C to +125°C | Power Dissipation | 1.0W |
| Storage Temperature | -65°C to +150°C | Lead Temperature (Soldering, 10 Seconds) | 300°C |
| All Input Voltages with Respect to Ground (Note 10) | +6.5V to -0.6V | V _{CC} Supply Voltage with Respect to Ground | +7.0V to -0.6V |
| All Output Voltages with Respect to Ground (Note 10) | V _{CC} + 1.0V to GND - 0.6V | Operating Conditions (Note 7) | |
| V _{PP} Supply Voltage with Respect to Ground during Programming | +14.0V to -0.6V | Temperature Range (T _{case}) | -55°C to +125°C |
| | | V _{CC} Power Supply | 5V ±10% |

READ OPERATION

DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------|--|--|------|-----|---------------------|-------|
| I _{LI} | Input Load Current | V _{IN} = V _{CC} or GND | | | 10 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = V _{CC} or GND, $\overline{CE} = V_{IH}$ | | | 10 | μA |
| I _{CC1} (Note 9) | V _{CC} Current (Active) TTL Inputs | $\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V _{IH} or V _{IL} , I/O = 0 mA | | 5 | 20 | mA |
| I _{CC2} (Note 9) | V _{CC} Current (Active) CMOS Inputs | $\overline{CE} = GND$, f = 5 MHz Inputs = V _{CC} or GND, I/O = 0 mA | | 3 | 10 | mA |
| I _{CCSB1} | V _{CC} Current (Standby) TTL Inputs | $\overline{CE} = V_{IH}$ | | 0.1 | 1 | mA |
| I _{CCSB2} | V _{CC} Current (Standby) CMOS Inputs | $\overline{CE} = V_{CC}$ | | 0.5 | 100 | μA |
| I _{PP} | V _{PP} Load Current | V _{PP} = V _{CC} | | | 200 | μA |
| V _{IL} | Input Low Voltage | | -0.1 | | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | | V _{CC} + 1 | V |
| V _{OL1} | Output Low Voltage | I _{OL} = 2.1 mA | | | 0.45 | V |
| V _{OH1} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | | V |
| V _{OL2} | Output Low Voltage | I _{OL} = 0 μA | | | 0.1 | V |
| V _{OH2} | Output High Voltage | I _{OH} = 0 μA | 4.4 | | | V |

AC Electrical Characteristics

| Symbol | Parameter | Conditions | 27C256 | | | | | | Units |
|------------------|---|--|--------|-----|-----|-----|-----|-----|-------|
| | | | 250 | | 300 | | 350 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| t _{ACC} | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 250 | | 300 | | 350 | ns |
| t _{CE} | \overline{CE} to Output Delay | $\overline{OE} = V_{IL}$ | | 250 | | 300 | | 350 | ns |
| t _{OE} | \overline{OE} to Output Delay | $\overline{CE} = V_{IL}$ | | 100 | | 120 | | 120 | ns |
| t _{DF} | \overline{OE} High to Output Float | $\overline{CE} = V_{IL}$ | 0 | 60 | 0 | 105 | 0 | 105 | ns |
| t _{OH} | Output Hold from Addresses, \overline{CE} or \overline{OE} , Whichever Occurred First | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

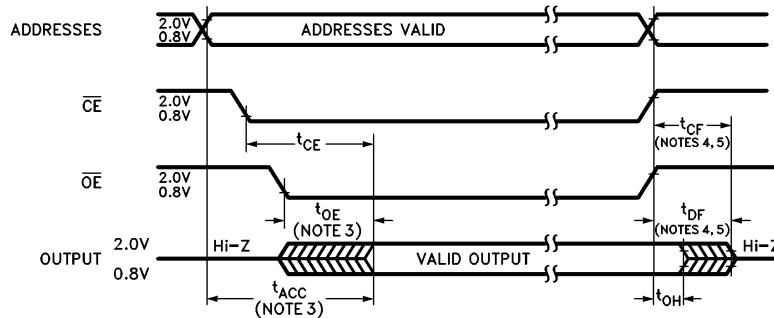
Capacitance $T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$ (Note 2)

| Symbol | Parameter | Conditions | Typ | Max | Units |
|-----------|--------------------|-----------------------|-----|-----|-------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{V}$ | 6 | 10 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0\text{V}$ | 9 | 14 | pF |

AC Test Conditions

| | | | |
|---------------------------|--|---|----------------------------|
| Output Load | 1 TTL Gate and $C_L = 100\text{ pF}$ (Note 8) | Timing Measurement Reference Level Inputs Outputs | 0.8V and 2V 0.8V and 2V |
| Input Rise and Fall Times | $\leq 5\text{ ns}$ | | |
| Input Pulse Levels | 0.45V to 2.4V | | |

AC Waveforms (Notes 6, 7 and 9)



TL/D/10332-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without impacting t_{ACC} .

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using \overline{OE} or \overline{CE} .

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0\text{V}$ to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6\text{ mA}$, $I_{OH} = -400\text{ }\mu\text{A}$.

C_L : 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 and 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|--|---|------|------|------|-------------|
| t_{AS} | Address Setup Time | | 2 | | | μs |
| t_{OES} | \overline{OE} Setup Time | | 2 | | | μs |
| t_{VPS} | V_{PP} Setup Time | | 2 | | | μs |
| t_{VCS} | V_{CC} Setup Time | | 2 | | | μs |
| t_{DS} | Data Setup Time | | 2 | | | μs |
| t_{AH} | Address Hold Time | | 0 | | | μs |
| t_{DH} | Data Hold Time | | 2 | | | μs |
| t_{DF} | Output Enable to Output Float Delay | $\overline{CE} = V_{IL}$ | 0 | | 130 | ns |
| t_{PW} | Program Pulse Width | | 0.5 | 0.5 | 10 | ns |
| t_{OE} | Data Valid from \overline{OE} | $\overline{CE} = V_{IL}$ | | | 150 | ns |
| I_{PP} | V_{PP} Supply Current during Programming Pulse | $\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$ | | | 30 | mA |
| I_{CC} | V_{CC} Supply Current | | | | 10 | mA |
| T_A | Temperature Ambient | | 20 | 25 | 30 | $^{\circ}C$ |
| V_{CC} | Power Supply Voltage | | 5.75 | 6.0 | 6.25 | V |
| V_{PP} | Programming Supply Voltage | | 12.2 | 13.0 | 13.3 | V |
| t_{FR} | Input Rise, Fall time | | 5 | | | ns |
| V_{IL} | Input Low Voltage | | | 0.0 | 0.45 | V |
| V_{IH} | Input High Voltage | | 2.4 | 4.0 | | V |
| t_{IN} | Input Timing Reference Voltage | | 0.8 | 1.5 | 2.0 | V |
| t_{OUT} | Output Timing Reference Voltage | | 0.8 | 1.5 | 2.0 | V |

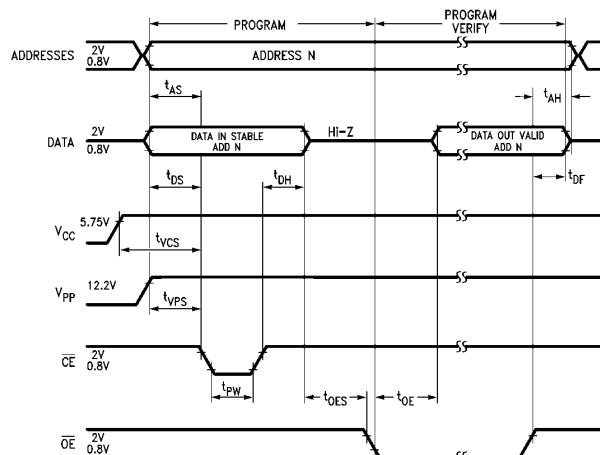
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} . The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC} .

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP} , V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms (Note 3)



TL/D/10332-4

Interactive Programming Algorithm Flow Chart

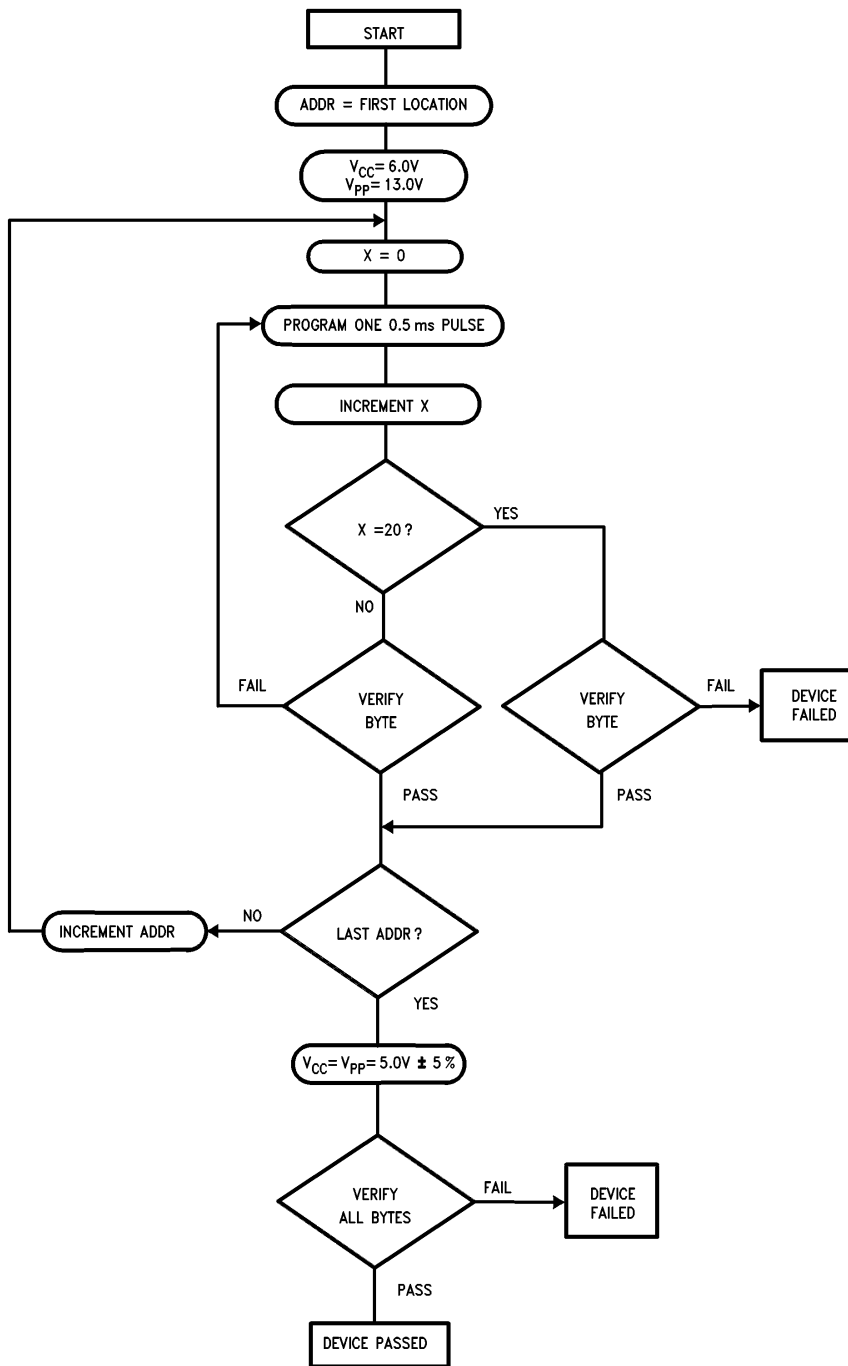


FIGURE 1

TL/D/10332-5

Functional Description

DEVICE OPERATION

The six modes of operation of the 27C256 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP} . The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The 27C256 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The 27C256 is placed in the standby mode by applying a CMOS high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Output OR-Tying

Because 27C256s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that \overline{CE} (pin 20) be decoded and used as the primary device selecting function, while \overline{OE} (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP} will damage the 27C256.

Initially, and after each erasure, all bits of the 27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27C256 is in the programming mode when the V_{PP} power supply is at 13.0V and \overline{OE} is at V_{IH} . It is required that at least a 0.1 μ F capacitor be placed across V_{PP} , V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the \overline{CE}/PGM input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The 27C256 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The 27C256 must not be programmed with a DC signal applied to the \overline{CE}/PGM input.

Programming multiple 27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the \overline{CE}/PGM input programs the paralleled 27C256s.

TABLE I. Mode Selection

| Mode | Pins | \overline{CE}/PGM (20) | \overline{OE} (22) | V_{PP} (1) | V_{CC} (28) | Outputs (11–13, 15–19) |
|-----------------|------|-----------------------------|-------------------------|-----------------|------------------|---------------------------|
| Read | | V_{IL} | V_{IL} | 5V | 5V | D_{OUT} |
| Standby | | V_{IH} | Don't Care | 5V | 5V | Hi-Z |
| Program | | V_{IL} | V_{IH} | 13.0V | 6V | D_{IN} |
| Program Verify | | V_{IH} | V_{IL} | 13.0V | 6V | D_{OUT} |
| Program Inhibit | | V_{IH} | V_{IH} | 13.0V | 6V | Hi-Z |
| Output Disable | | Don't Care | V_{IH} | 5V | 5V | Hi-Z |

Functional Description (Continued)

Program Inhibit

Programming multiple 27C256s in parallel with different data is also easily accomplished. Except for \overline{CE} all like inputs (including \overline{OE}) of the parallel 27C256s may be common. A TTL low level program pulse applied to an 27C256's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 13.0V will program that 27C256. A TTL high level \overline{CE} input inhibits the other 27C256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC} , except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C256 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 \AA –4000 \AA range.

After programming, opaque labels should be placed over the 27C256's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the 27C256 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of 15W-sec/cm².

The 27C256 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their

tubes which should be removed before erasure. Table II shows the minimum 27C256 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

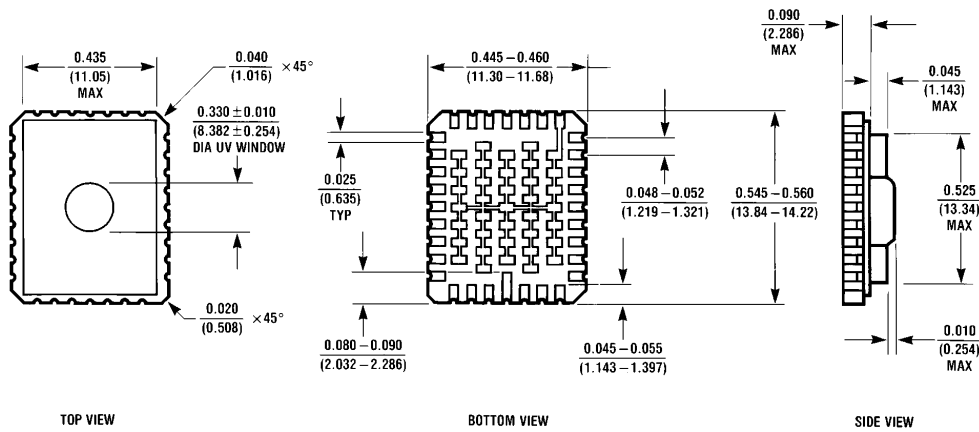
SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum 27C256 Erasure Time

| Light Intensity (Micro/Watts/cm ²) | Erasure Time (Minutes) |
|---|---------------------------|
| 15,000 | 20 |
| 10,000 | 25 |
| 5,000 | 50 |

Physical Dimensions inches (millimeters)

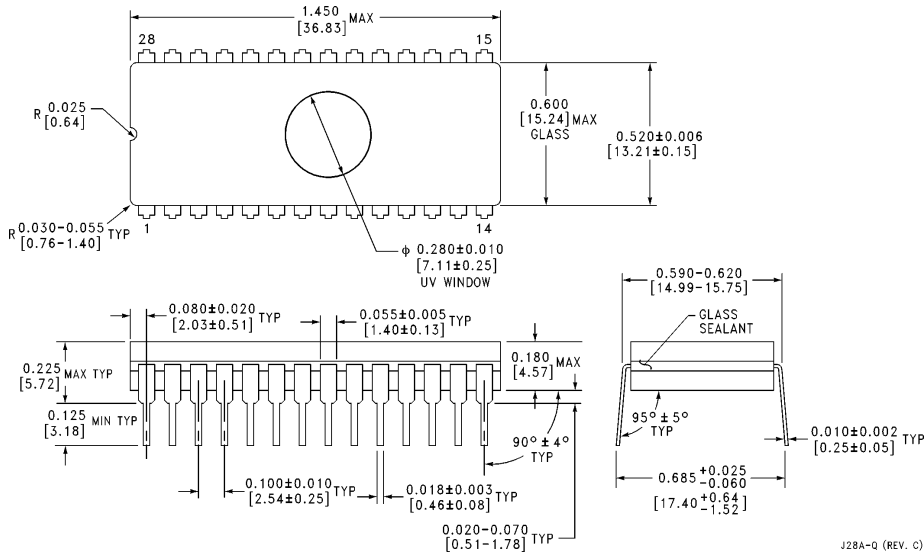


EA32CQ (REV A)

32L Leadless Chip Carrier (E)
Order Number 27C256E350/883, 27C256E300/883, 27C256E250/883
NS Package Number EA32CQ

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114730



28 Lead EPROM Dual-In-Line Cerdip Package (JQ) Small Window
Order Number 27C256Q350/883, 27C256Q300/883, 27C256Q250/883
NS Package Number J28AQ

J28A-Q (REV. C)

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