

# DATA SHEET

## **74ALS74A**

Dual D-type flip-flop with set and reset

Product specification

1996 Jul 01

IC05 Data Handbook

# Dual D-type flip-flop with set and reset

# 74ALS74A

## DESCRIPTION

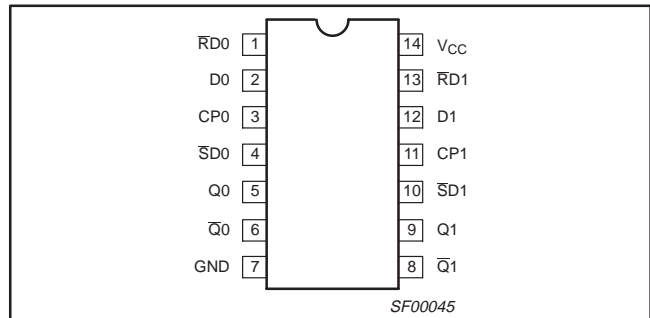
The 74ALS74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) are asynchronous active-Low inputs and operate independently of the clock input. When set and reset are inactive (High), data at the D input is transferred to the Q and  $\overline{Q}$  outputs on the Low-to-High transition of the clock. Data must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS74A	150MHz	3.0mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
14-pin plastic DIP	74ALS74AN	SOT27-1
14-pin plastic SO	74ALS74AD	SOT108-1
14-pin plastic SSOP Type II	74ALS74ADB	SOT337-1

## PIN CONFIGURATION

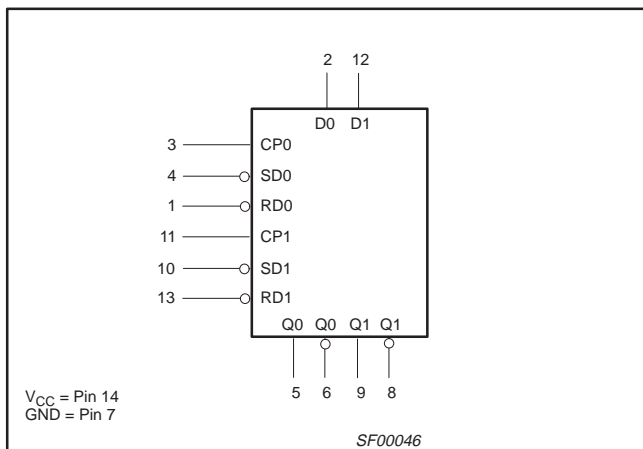


## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

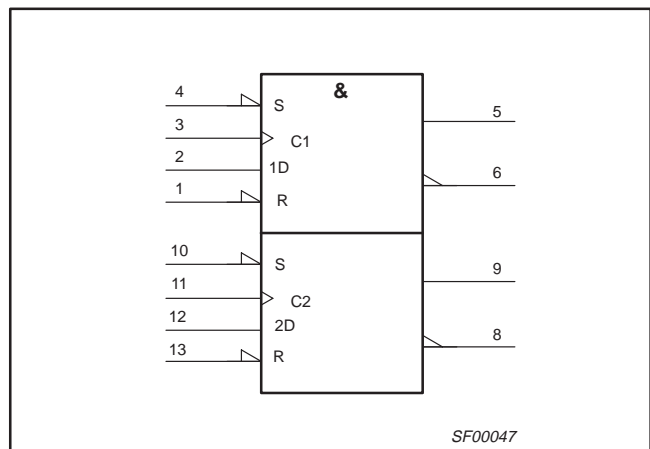
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0, D1	Data inputs	1.0/2.0	20 $\mu$ A/0.2mA
CP0, CP1	Clock inputs (active rising edge)	1.0/2.0	20 $\mu$ A/0.2mA
$\overline{SD}$ 0, $\overline{SD}$ 1	Set inputs (active-Low)	2.0/4.0	40 $\mu$ A/0.4mA
$\overline{RD}$ 0, $\overline{RD}$ 1	Reset inputs (active-Low)	2.0/4.0	40 $\mu$ A/0.4mA
Q0, Q1, $\overline{Q}$ 0, $\overline{Q}$ 1	Data outputs	20/80	0.4mA/8mA

**NOTE:** One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

## LOGIC SYMBOL



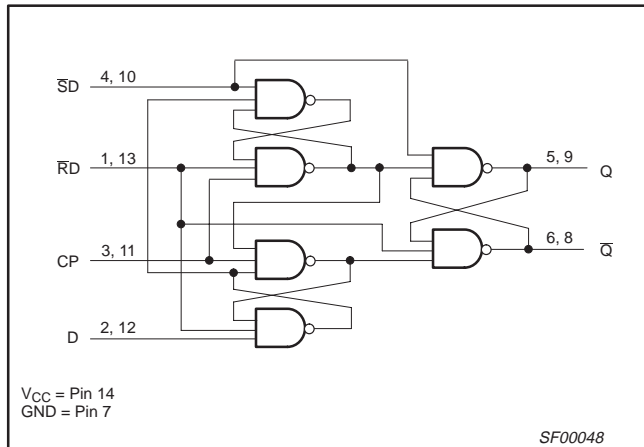
## IEC/IEEE SYMBOL



# Dual D-type flip-flop with set and reset

# 74ALS74A

## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↑	X	NC	NC	Hold

H = High voltage level  
 h = High state must be present one setup time prior to Low-to-High clock transition  
 L = Low voltage level  
 l = Low state must be present one setup time prior to Low-to-High clock transition  
 NC = No change from the previous setup  
 X = Don't care  
 ↑ = Low-to-High clock transition  
 ↑ = Not Low-to-High clock transition  
 \* = Both outputs will be High while both  $\overline{SD}$  and  $\overline{RD}$  are Low, but the output states are unpredictable if  $\overline{SD}$  and  $\overline{RD}$  go High simultaneously

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	16	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{ik}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-0.4	mA
$I_{OL}$	Low-level output current			8	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

## Dual D-type flip-flop with set and reset

74ALS74A

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT	
					MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = ±10%, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = MAX	V <sub>CC</sub> - 2			V	
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN		I <sub>OL</sub> = 4mA		0.25	0.40	V
					I <sub>OL</sub> = 8mA		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.5	V	
I <sub>I</sub>	Input current at maximum input voltage	Dn, CPn	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				0.1	mA	
		$\overline{S}$ Dn, $\overline{R}$ Dn					0.2	mA	
I <sub>IH</sub>	High-level input current	Dn, CPn	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA	
		$\overline{S}$ Dn, $\overline{R}$ Dn					40	μA	
I <sub>IL</sub>	Low-level input current	Dn, CPn	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V				-0.2	mA	
		$\overline{S}$ Dn, $\overline{R}$ Dn					-0.4	mA	
I <sub>O</sub>	Output current <sup>3</sup>		V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.25V		-30		-112	mA	
I <sub>CC</sub>	Supply current (total) <sup>4</sup>		V <sub>CC</sub> = MAX			3.0	4.0	mA	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.
- Measure I<sub>CC</sub> with the Dn, CPn, and  $\overline{S}$ Dn grounded, then with Dn, CPn, and  $\overline{R}$ Dn grounded.

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	MAX	
f <sub>max</sub>	Maximum clock frequency		Waveform 1	80		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CPn to Qn or $\overline{Q}$ n		Waveform 1	3.0	14.0	ns
				3.0	14.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\overline{S}$ Dn or $\overline{R}$ Dn to Qn or $\overline{Q}$ n		Waveform 2, 3	1.0	8.0	ns
				3.0	10.0	

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	MAX	
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, High or Low Dn to CPn		Waveform 1	6.0 6.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low Dn to CPn		Waveform 1	0.0 0.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CPn Pulse width High or Low		Waveform 1	6.0 6.0		ns
t <sub>w</sub> (L)	$\overline{S}$ Dn or $\overline{R}$ Dn Pulse width, Low		Waveform 2, 3	6.0		ns
t <sub>rec</sub>	Recovery time, $\overline{S}$ Dn or $\overline{R}$ Dn to CPn		Waveform 2, 3	6.0		ns

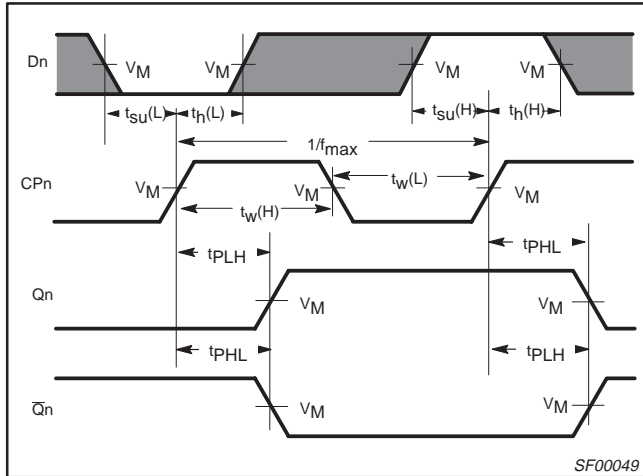
# Dual D-type flip-flop with set and reset

# 74ALS74A

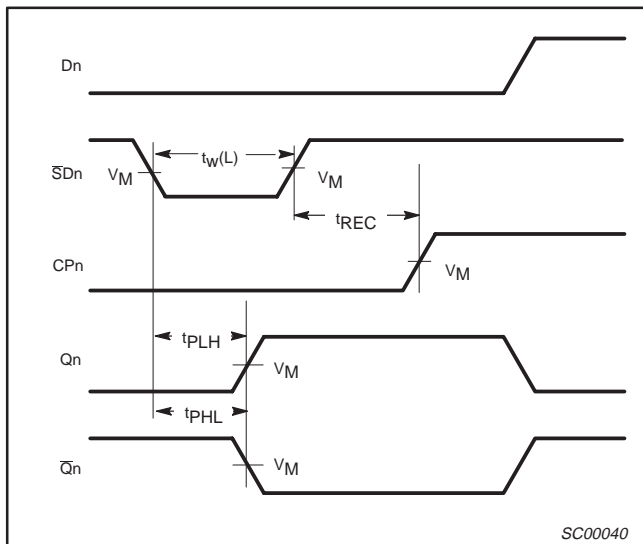
## AC WAVEFORMS

For all waveforms,  $V_M = 1.3V$ .

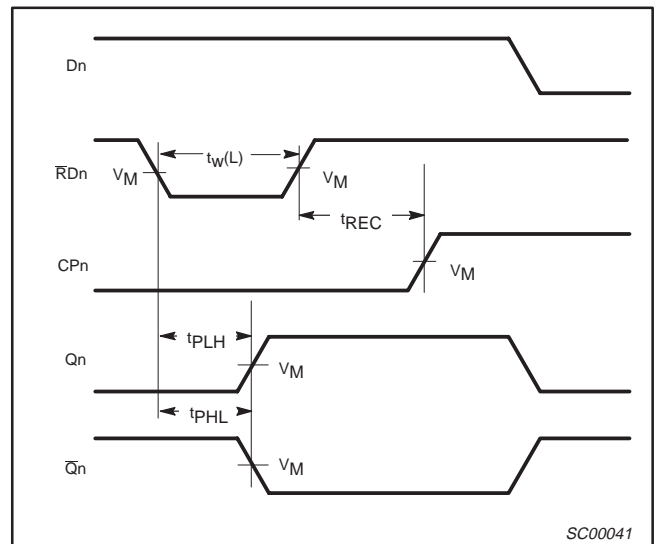
The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 1. Propagation Delay for Data to Output, Data Setup and Hold Times, Clock Width, and Maximum Clock Frequency**



**Waveform 2. Propagation Delay for Set to Output, Set Pulse Width and Recovery Time for Set to Clock**

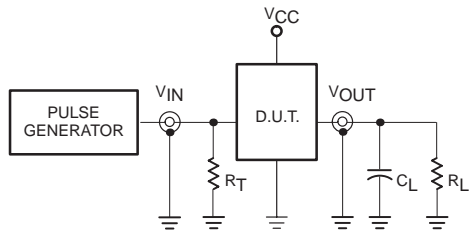


**Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width and Recovery Time for Reset to Clock**

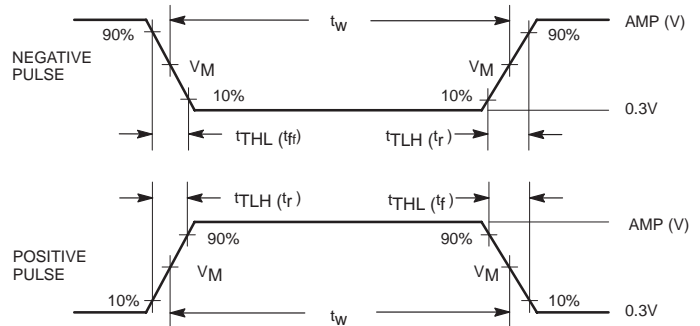
# Dual D-type flip-flop with set and reset

# 74ALS74A

## TEST CIRCUIT AND WAVEFORMS



**Test Circuit for Totem-pole Outputs**



**Input Pulse Definition**

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	$V_M$	Rep.Rate	$t_w$	$t_{TLH}$	$t_{THL}$
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00005

## Dual D-type flip-flop with set and reset

74ALS74A

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## LIFE SUPPORT APPLICATIONS

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

**Philips Semiconductors**  
**811 East Arques Avenue**  
**P.O. Box 3409**  
**Sunnyvale, California 94088-3409**  
**Telephone 800-234-7381**

© Copyright Philips Electronics North America Corporation 1997  
 All rights reserved. Printed in U.S.A.

*Let's make things better.*

---

Dual D-type flip-flop with set and reset

74ALS74A

---

**DIP14:** plastic dual in-line package; 14 leads (300 mil)

**SOT27-1**



---

Dual D-type flip-flop with set and reset

74ALS74A

---

**SO14:** plastic small outline package; 14 leads; body width 3.9 mm

**SOT108-1**

---

Dual D-type flip-flop with set and reset

74ALS74A

---

**NOTES**